

WHAT IS CLAIMED IS:

1 1. A level shifter comprising:
2 a first transistor connected between a first power source
3 line and an output node;
4 a second transistor connected between the output node and
5 a second power source line;
6 a third transistor connected between the first power source
7 line and the output node;
8 a fourth transistor connected between the output node and
9 the second power source line; and
10 a control circuit that causes the second transistor and
11 the fourth transistor to turn on when an input signal is of a
12 first level and causes the third transistor and the first
13 transistor to turn on when the input signal is of a second level
14 different from the first level,
15 wherein a gate tolerant voltage of the first transistor
16 is smaller than a gate tolerant voltage of the third transistor,
17 and a gate tolerant voltage of the fourth transistor is smaller
18 than a gate tolerant voltage of the second transistor.

1 2. A level shifter according to claim 1, wherein the control
2 circuit comprises:
3 a fifth transistor which is connected between the first
4 power source line and a first node, a gate thereof being connected
5 with the output node;
6 a sixth transistor which is connected between the first
7 node and the second power source line, in which a gate thereof
8 receives the input signal;

9 a seventh transistor which is connected between the first
10 power source line and a second node, in which a gate thereof
11 receives the input signal; and

12 an eighth transistor which is connected between the second
13 node and the second power source line, a gate thereof being
14 connected with the output node.

1 3. A level shifter according to claim 2, wherein the control
2 circuit further comprises an inverter circuit that produces an
3 inverted input signal, a polarity of which being inverted, and
4 supplies the inverted input signal to a gate of the second
5 transistor and a gate of the third transistor.

1 4. A level shifter according to claim 2, wherein each of
2 the first, fourth, fifth, and eighth transistors has a first
3 gate tolerant voltage, and each of the second, third, sixth,
4 and seventh transistors has a second gate tolerant voltage.

1 5. A level shifter according to claim 1, wherein each of
2 the second and third transistors operates in a non-saturation
3 region.

1 6. A level shifter according to claim 1, wherein the control
2 circuit

3 causes the second transistor to turn on before turning
4 on the fourth transistor when the input signal is of the first
5 level and

6 causes the third transistor to turn on before turning on

7 the first transistor when the input signal is of the second level.

1 7. A level shifter according to claim 1, wherein a current
2 supply capacity of the first transistor is larger than a current
3 supply capacity of the third transistor and a current supply
4 capacity of the fourth transistor is larger than a current supply
5 capacity of the second transistor.

1 8. A level shifter according to claim 1, wherein the gate
2 tolerant voltage of the first transistor and the gate tolerant
3 voltage of the fourth transistor are equal to a voltage amplitude
4 of an output signal outputted to the output node.

1 9. A level shifter according to claim 1, wherein the gate
2 tolerant voltage of the second transistor and the gate tolerant
3 voltage of the third transistor are equal to a voltage amplitude
4 of an input signal.

1 10. A level shifter according to claim 2, wherein the first
2 node and the second node are electrically connected with each
3 other.

1 11. A level shifter according to claim 1, wherein the first
2 transistor and the fourth transistor each are formed from a
3 transistor that operates in a saturation region at a first speed
4 and has a first current supply capacity, and the second transistor
5 and the third transistor each are formed from a transistor that
6 operates in a non-saturation region at a second speed lower than

7 the first speed and has a second current supply capacity lower
8 than the first current supply capacity.

1 12. A level shifter comprising:

2 a first transistor of a first conductivity type having
3 a first gate tolerant voltage, which is connected between a first
4 power source line and a first node, in which a gate thereof receives
5 an input signal;

6 a second transistor of a second conductivity type having
7 a second gate tolerant voltage smaller than the first gate
8 tolerant voltage, which is connected between a second power
9 source line and a second node, in which a gate thereof is connected
10 with the first node;

11 a third transistor of the first conductivity type having
12 the first gate tolerant voltage, which is connected between the
13 second node and the first power source line, in which a gate
14 thereof receives an inverted input signal of the input signal;

15 a fourth transistor of the second conductivity type having
16 the first gate tolerant voltage, which is connected between the
17 second power source line and a third node, in which a gate thereof
18 receives the input signal;

19 a fifth transistor of the second conductivity type having
20 the second gate tolerant voltage, which is connected between
21 the second power source line and the second node, in which a
22 gate thereof receives the inverted input signal; and

23 a sixth transistor of the first conductivity type having
24 the second gate tolerant voltage, which is connected between
25 the second node and the first power source line, in which a gate

26 thereof is connected with the third node.

1 13. A level shifter according to claim 12, further
2 comprising:

3 a seventh transistor of the second conductivity type having
4 the second gate tolerant voltage, which is connected between
5 the first node and the second power source line, in which a gate
6 thereof is connected with the second node; and

7 an eighth transistor of the first conductivity type having
8 the second gate tolerant voltage, which is connected between
9 the third node and the first power source line, in which a gate
10 thereof is connected with the second node.

1 14. A level shifter according to claim 13, wherein the
2 first node and the third node are electrically connected with
3 each other.

1 15. A level shifter comprising:

2 a first transistor of a first conductivity type, which
3 is connected between a first power source line and a first node,
4 in which a control terminal thereof is connected with a second
5 node;

6 a second transistor of the first conductivity type, which
7 is connected between the first power source line and the second
8 node, in which a control terminal thereof is connected with the
9 first node;

10 a third transistor of a second conductivity type, which
11 is connected between the first node and a second power source

12 line, in which a control terminal thereof receives an input
13 signal;

14 a fourth transistor of the second conductivity type, which
15 is connected between the second node and the second power source
16 line, in which a control terminal thereof receives an inverted
17 input signal of the input signal;

18 a fifth transistor of the first conductivity type, which
19 is connected between the first power source line and the second
20 node, in which a control terminal thereof receives the inverted
21 input signal;

22 a sixth transistor of the second conductivity type, which
23 is connected between the second node and the second power source
24 line, in which a control terminal thereof is connected with a
25 third node;

26 a seventh transistor of the first conductivity type, which
27 is connected between the first power source line and the third
28 node, in which a control terminal thereof receives the input
29 signal; and

30 an eighth transistor of the second conductivity type, which
31 is connected between the third node and the second power source
32 line, in which a control terminal thereof is connected with the
33 second node,

34 wherein each of the first, second, sixth, and eighth
35 transistors operates in a saturation region in accordance with
36 a level of the input signal, and each of the third, fourth, fifth,
37 and seventh transistors operates in a non-saturation region
38 independently of the level of the input signal.